

REMARKS

Claims 3, 6 and 22-23 have been cancelled. Claims 1, 4-5, 7, 20-21, 26 and 28-29 have been amended and claim 30 has been added. Claims 1, 4-5, 6-21 and 24-30 remain for further consideration. No new matter has been added.

The objections and rejections shall be taken up in the order presented in the Official Action.

1-4. Claim 22 currently stands objected for allegedly being a substantial duplicate of claim 20.

Claim 22 has been cancelled.

5-6. Claims 6 and 23 currently stand rejected for allegedly failing to comply with the enablement requirement.

Claims 6 and 23 have been cancelled.

7-8. Claims 21, 26, 28 and 29 currently stand rejected for allegedly being indefinite for failing to point out and distinctly claim the subject matter deemed to be the present invention.

Claims 21, 26, 28 and 29 have been amended.

9. Claims 1, 3, 5-10 and 20-29 currently stand rejected for allegedly being anticipated by U.S. Patent 6,584,528 to Kurafuji (hereinafter “Kurafuji”).

Claim 1

Amended claim 1 recites a storage device for a multibus architecture. The storage device includes:

“at least one memory that stores information;

a memory connection having a port that is connected to the at least one memory and is selectively connected to one of a plurality of buses within the multibus architecture, at least one data line that communicates with the memory connection and the one of the plurality of buses to provide information to the memory connection to control the memory;

a switching device that selectively connects the memory connection to one of the plurality of buses to transmit information between the one of the plurality of buses and the memory; and

an analyzer that analyzes addresses on address lines which form a part of at least one of the plurality of buses for determining a selective access to the at least one memory by one of the plurality of buses, where the analyzer comprises an access control device that switches the switching device and a comparator that compares an address on one of the plurality of buses with a memory address of the at least one memory and controls the access control device to control the switching device as a function of the result of the comparison.” (emphasis added, cl. 1)

Claim 1 has been amended, in part, to include certain features of claims 3 and 6, now cancelled. Kurafuji fails to anticipate amended claim 1 because Kurafuji fails to disclose at least the features of amended claim 1 emphasized above. Regarding former claim 6, the Official Action contends that Kurafuji disclosed “*one comparator per each one of the plurality of buses to compare the address with the memory address of the at least one memory (col. 2, line 63 – col. 3, line 7 and col. 5, lines 48-54, detects matching address inherently teaches comparator to match address.*” (Official Action, pg. 5). However, the portion of Kurafuji cited at col. 2, line 63 to col. 3, line 7

discloses that the selector circuit handles simultaneous access requests to the same memory bank on the first and second buses by generating an exception signal to the processor in order to arbitrate these simultaneous requests. Kurafuji discloses that these simultaneous access requests *“can be arbitrated by an exception handling program performed on the processor core.”* (Col. 3, lines 4-5). This disclosure in Kurafuji fails to teach or suggest the features of amended claim 1 emphasized above (e.g., the comparison of the bus address with the memory address and the control of the switching device as a result of the comparison), as the cited portion of Kurafuji deals solely with arbitrating simultaneous accesses to the same memory bank and not with such specific comparison and switching device control features of the claimed invention. Thus, there is no disclosure or suggestion in this cited portion of Kurafuji regarding the arbitration of simultaneous memory access of any of the emphasized features of amended claim 1; specifically, *“an access control device that switches the switching device and at least one comparator that compares an address on one of the plurality of buses with a memory address of the at least one memory and controls the access control device to control the switching device as a function of the result of the comparison.”*

Further, the second cited location in the Official Action of Kurafuji at col. 5, lines 48-54 discloses *“a mode register address detecting portion 61 that receives data address 72, and outputs a mode register address detecting signal 97 when it detects matching of the received data address 72 and an address allocated to mode register 20.”* The Official Action contends that this cited location in Kurafuji *“detects matching address inherently teaches comparator to match address.”* (Official Action, pg. 5). This disclosure in Kurafuji relates to the provision of a signal 97 when a bus address matches an address “allocated” to a mode register 20. There is no disclosure or suggestion in Kurafuji that an address of a memory is allocated to the mode register

20. Instead, a fair reading of Kurafuji is that the mode register 20 has its own address, and not a memory address, “allocated” to it. Indeed, the mode register 20 is not disclosed in Kurafuji to be a part of any of the memory devices which would have corresponding memory addresses assigned to them. In addition, the alleged “matching” of the addresses does not necessarily inherently disclose the use of a comparator to carry out the matching. However, even assuming that the contention in the Official Action that “*detects matching address inherently teaches comparator to match address*” does involve a comparator without admitting as much, the cited location of Kurafuji at col. 5, lines 48-54 still fails to disclose at least the memory address comparison feature and the resulting switching device control feature of amended claim 1; specifically, “*an access control device that switches the switching device and at least one comparator that compares an address on one of the plurality of buses with a memory address of the at least one memory and controls the access control device to control the switching device as a function of the result of the comparison.*”

In light of the foregoing, Kurafuji fails to anticipate amended claim 1. As a result, it is respectfully submitted that the anticipation rejection of amended claim 1 is moot and should be removed, and that amended claim 1 is in condition for allowance and should be passed to issuance.

Claim 20

Amended claim 20 recites a storage device for use with a bus architecture having a plurality of buses including address, data and control information transmitted on the plurality of buses. The storage device includes:

“a memory;

a switching device that selectively connects the memory with one of the plurality of buses to transmit information on the selected one of the plurality of buses to the memory;

a logic device that provides an interrupt signal on a line to a processor to interrupt operation of the processor whenever an access to the memory is desired by at least one of the plurality of buses; and

an analyzer that analyzes an address on address lines that form a portion of at least one of the plurality of buses, where the analyzer controls the switching device to selectively connect one of the plurality of buses to the memory depending on the address that is analyzed by the analyzer, where the analyzer further comprises an access control device that switches the switching device and at least one comparator that compares an address on one of the plurality of buses with a memory address of the memory and controls the access control device to control the switching device as a function of the result of the comparison.” (cl. 20)

Claim 20 has been amended, in part, to include certain features of claims 6 and 23, now cancelled. Therefore, the discussion above with respect to the patentability of amended claim 1 is equally applicable to amended claim 20.

As a result, it is respectfully submitted that the anticipation rejection of amended claim 20 is moot and should be removed, and that amended claim 20 is in condition for allowance and should be passed to issuance.

Claim 29

Since original claim 29 currently stands rejected for the same reasons as original claim 20, and since claim 29 has been amended similar to amended claim 20, the arguments above with respect to the patentability of amended claim 29 apply equally as well to amended claim 29.

As a result, it is respectfully submitted that the anticipation rejection of amended claim 29 is moot and should be removed, and that amended claim 29 is in condition for allowance and should be passed to issuance.

10-11. Claim 2 currently stands rejected for allegedly being obvious in view of the combined subject matter disclosed in Kurafuji, U.S. Published Application 2004/0059897 to Rogers, and U.S. Patent 6,789,150 to Jain.

It is respectfully submitted that the rejection of this claim is now moot, since claim 2 depends directly from amended claim 1, which is patentable for at least the reasons set forth above.

12. Claim 4 currently stands rejected for allegedly being obvious in view of the combined subject matter disclosed in Kurafuji and U.S. Patent 6,138,204 to Amon.

It is respectfully submitted that the rejection of this claim is now moot, since claim 4 depends directly from amended claim 1, which is patentable for at least the reasons set forth above.

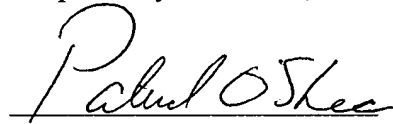
New Claim 30

Claim 30 has been added. It is respectfully submitted that claim 30 is patentable over the prior art of record, either alone or in combination since the claimed invention recites the feature of a programmable separator device that stores a memory address of the memory device for analysis by the analyzer.

For all the foregoing reasons, reconsideration and allowance of claims 1, 4-5, 6-21 and 24-30 is respectfully requested.

If a telephone interview could assist in the prosecution of this application, please call the undersigned attorney.

Respectfully submitted,

A handwritten signature in cursive script, reading "Patrick O'Shea", written over a horizontal line.

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